Run IIb Event Builder Upgrade

Motivation

Plan

Status

Bruce Knuteson (MIT)
on behalf of Run IIb EVB group

http://www-cdf.fnal.gov/upgrades/run2b/Documents/tdr_sep02.pdf

Assumed luminosity was 4×10^{32}

Justification was high-p_T program

These triggers give 750 Hz

→ Rate spec is 1 kHz

Event size assumed to grow

→ Size spec is 500 kB

→ Throughput spec is

500 MB/sec

(many safety factors here)

Trigger	Rates at 4×10^{32} cm^{-2}s^{-1}		
	L1	L2	L3
e/μ	2,327 Hz	250 Hz	22 Hz
ν	4,401 Hz	130 Hz	9 Hz
calibration	2,940 Hz	117 Hz	16 Hz
Total	9,668 Hz	497 Hz	47 Hz

Table 6.1: Summary of trigger rates for Higgs search triggers at $\mathcal{L} = 4 \times 10^{32}$ cm^{-2}s^{-1}. These triggers are important for many other high-p_T physics analyses.

Trigger	σ_{L1}(nb)	σ_{L2}(nb)	σ_{L3}(nb)
High-p_T jets	19,000	60	17
$t\bar{t}$ (all hadronic)	(overlap)	50	5
$\tau\bar{\tau}$	5,000	50	4
$\not\!\!E_T + \tau$	(overlap)	50	4
High-E_T photons	13,500	110	21
di,tri-leptons	1,000	190	45
Total	38,500	660	96
Total rate	15,400 Hz	264 Hz	38 Hz

Table 6.2: Summary of triggers necessary for the CDF Run IIb high-p_T physics program. The estimated rates shown are for an instantaneous luminosity of $\mathcal{L} = 4 \times 10^{32}$ cm^{-2}s^{-1}.

DØ has a system that runs at our spec (1 kHz, 250+ kB/event)

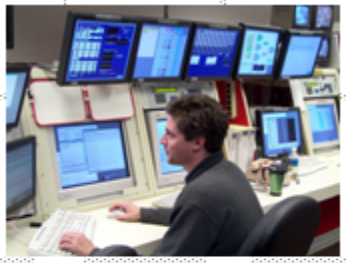
Put together in a year by a core team of ≈ 6 people

Made use of off the shelf, Ethernet-based hardware

CHEP03

Run II DZERO DAQ/ Level 3 Trigger System





Ron Rechenmacher, Fermilab

The DØ DAQ Group (Brown/FNAL-CD/U.of Washington)

Our strategy: Make use of a demonstrated, working solution to the same problem to implement a system appropriate for CDF

Core team:

Raphael Galea (MIT)

Bruce Knuteson (MIT)

Ron Rechenmacher (Fermilab)

Sham Sumorok (MIT)

Steve Tether (MIT)

Block design

No change to Level 3 subfarms

Modify converter node to GbE input

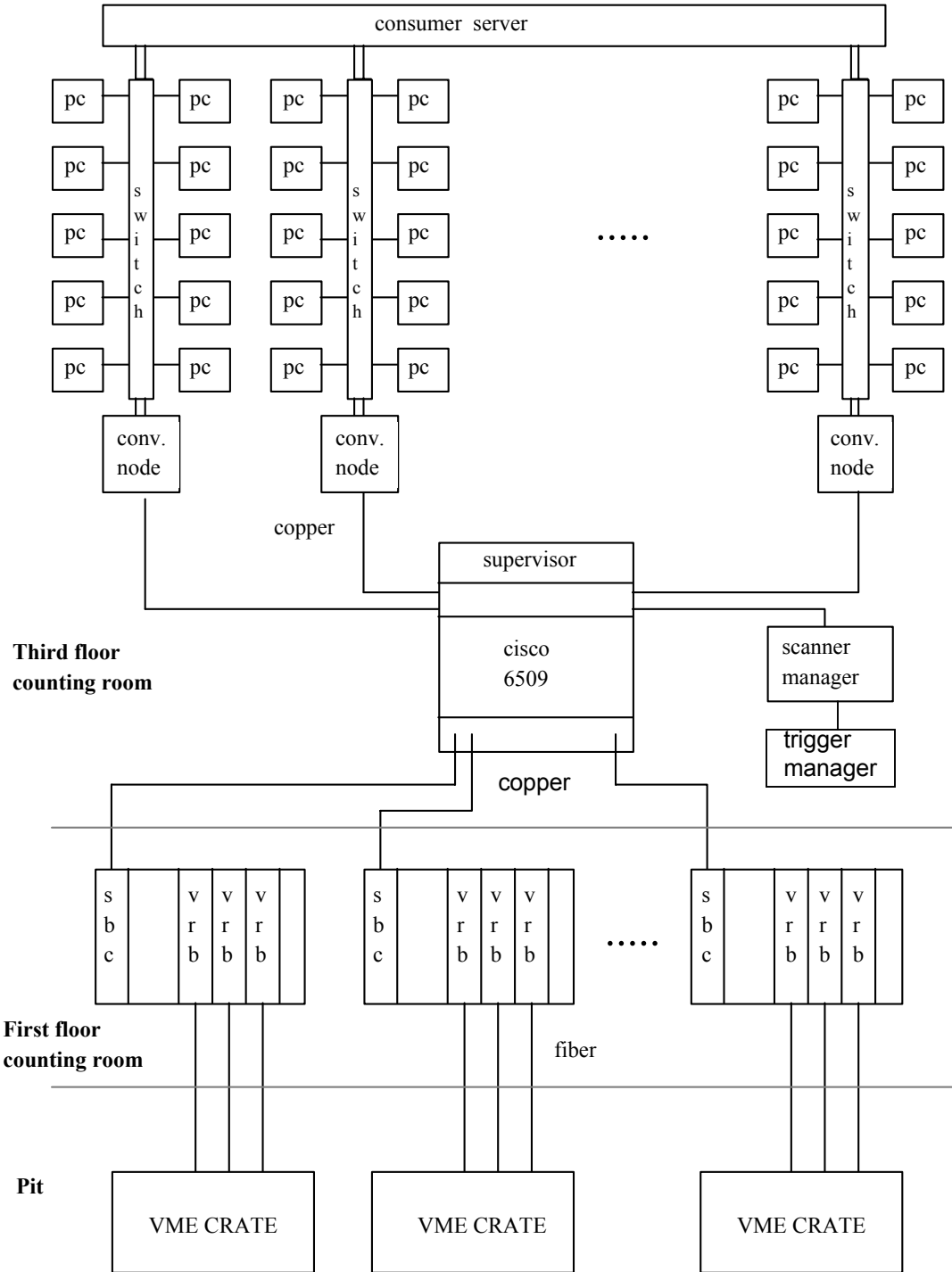
Replace existing ATM switch with gigabit Ethernet switch

Rewrite control software

Consider replacing control system (ScramNet → Ethernet)

New boards to read VME to GbE replace current SCPUs

No change to VRBs with exception of COT



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Data Sheet

Cisco Catalyst 6500 Series
Mixed Media Gigabit Ethernet Modules

The Cisco Catalyst® 6500 Series Switch—the premier modular multilayer switch—delivers secure converged services from the wiring closet to the core, to the data center, to the WAN edge.

Figure 1 Cisco Catalyst 6500 Series Gigabit Ethernet Interface Modules WS-X6724-SFP with optional (future availability) aCEF daughter card WS-F6700-AFC3

Fermilab standard

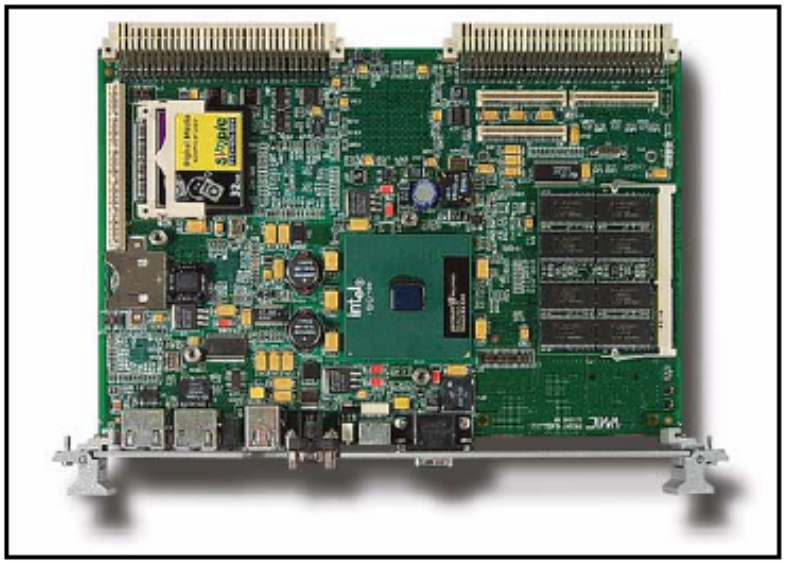
CD provides 24/7 support

P.O. out for switch to be used in final system

VMIC
A GE Fanuc Company

VMIVME-7805
Intel® Pentium® 4 Processor-M Based VMEbus Single-Board Computer

- Pentium® 4 Processor-M µFCPGA socket processor-based single-board computer (SBC) with 400 MHz system bus
- Special features for embedded applications include:
  - Up to 1 Gbyte bootable flash on secondary IDE (optional)
  - Two 16-bit and two 32-bit programmable timers
  - 32 Kbyte of nonvolatile SRAM
  - Software-selectable watchdog timer with reset
  - Remote Ethernet booting
  - PMC expansion site (IEEE-P1386 common mezzanine card standard, 5 V)
  - VME64 modes supported: A32/A24/D32/D16/D08(EO)/MBLT64/BLT32
  - VMEbus interrupt handler, interrupter and system controller
  - Includes real-time endian conversion hardware for little-endian and big-endian data interfacing (patent no. 6,032,212)
  - Enhanced bus error handling
  - Passive heat sink
- Standard features for embedded applications include:
  - Up to 2.20 GHz Pentium 4 Processor-M with 512 Kbyte advanced transfer cache
  - Up to 1 Gbyte PC2100 DDR SDRAM using two SODIMMs
  - Internal SVGA and DVI controller
  - 400 MHz system bus via Intel® 852GM chipset
  - One Ethernet controller supporting 10BaseT and 100BaseTX interfaces
  - One Ethernet controller supporting 10BaseT, 100BaseTX and 1000BaseT interfaces



Additional features within the Intel NetBurst mico-architecture include advanced dynamic execution.

of 8 ▸ ▸| 8.5 x 10.99 in

Single board computer to read VME into Cisco switch, replaces SCPU

Older version of this board used successfully in DØ system

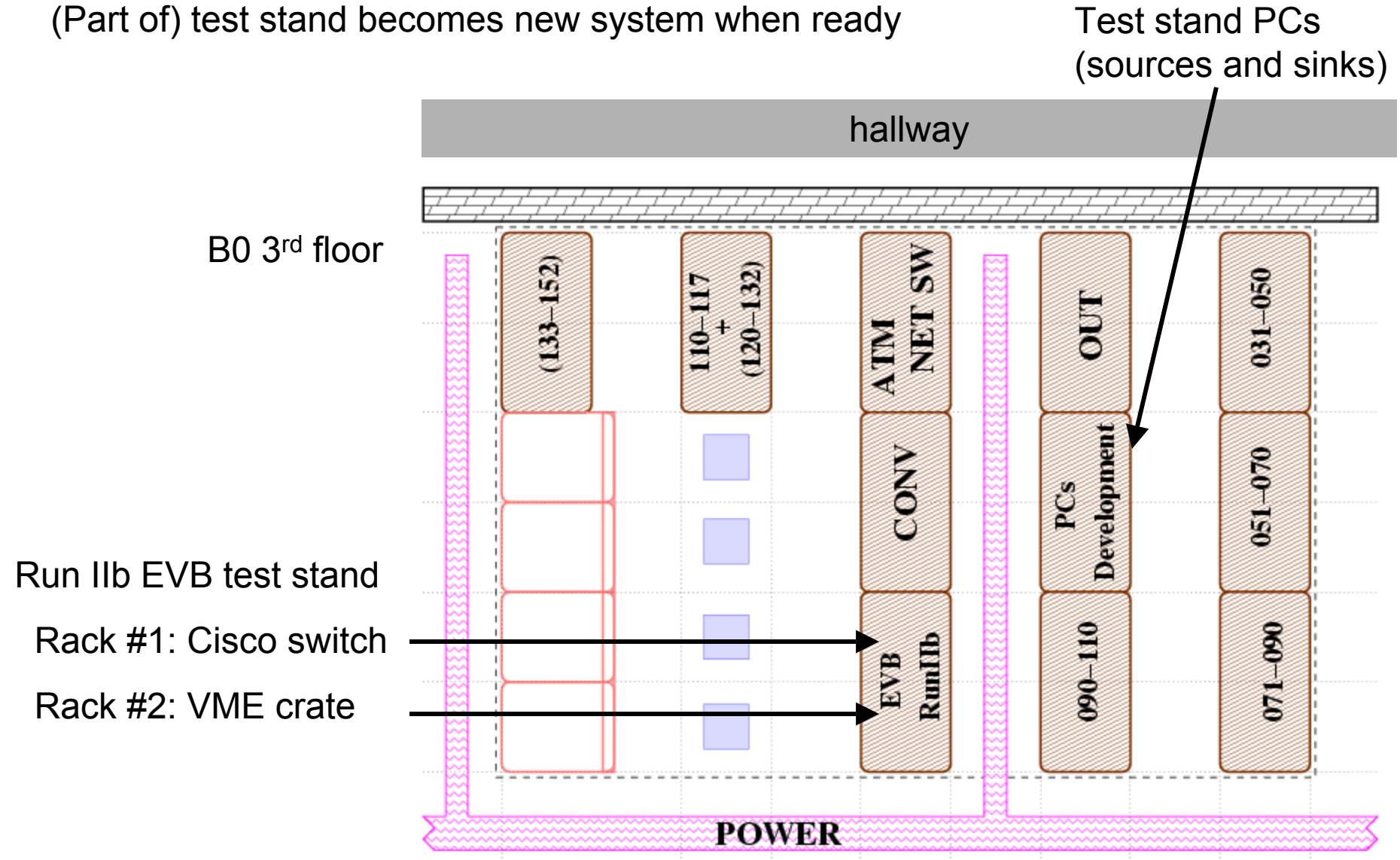
VxWorks → Linux

P.O.'s out for two boards to use in test stand

A test stand is being set up on B0 3rd floor

This stand will be used to develop the system

(Part of) test stand becomes new system when ready



WBS 1.3.4

Major milestones

1 July 2004	Working prototype system, functionality of new control software demonstrated
1 Nov 2004	P.O.’s out for remaining hardware
1 Mar 2005	Move to new system

http://mit.fnal.gov/~knuteson/papers/RunIIbEVB01_DesignOverviewProjectStatus.doc

Summary

Technology decision has been made (gigabit Ethernet)

Basic design has been decided

Upgrade interface boundaries very carefully drawn

- no change to Level 3
- no change to VRBs

Hardware for VME to switch readout has been selected, and initial boards ordered (VMIC 7805)

GbE switch has been selected, and final system switch ordered (Cisco 6509)

Expertise from DØ system is being incorporated (Rechenmacher)

Expertise from current CDF system is being used fully (Tether)

We expect to have a working prototype by 1 July 2004

functional new system by 1 Mar 2005